Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claim 1 (currently amended): In a processor, a method for performing computer graphics view volume clipping comparisons to determine if a vertex is located within a specified view volume, the method comprising:

transforming a plurality of coordinates representing the vertex into a plurality of transformed coordinates; and

using a floating point magnitude compare instruction to

~~perform a magnitude comparison between~~ determine an absolute value of at least one of the plurality of transformed coordinates and an absolute value that represents, for each respective at least one transformed coordinate, opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, and

perform a magnitude comparison between the absolute value of each of the at least one of the plurality of transformed coordinates and the absolute value of the corresponding view volume edges, wherein the magnitude comparison for each transformed coordinate involves a single comparison operation, and wherein comparison results for at least two view volume edges are obtained.

Claim 2 (previously presented): The method of Claim 1, wherein each of the at least one of the plurality of transformed coordinates are processed in parallel.

Claim 3 (previously presented): The method of Claim 1, further comprising:

setting a plurality of condition code bits to one or more specific states to indicate results of the magnitude comparison.

Claim 4 (previously presented): The method of Claim 1, further comprising:

specifying a compare condition in the floating point magnitude compare instruction.

Claim 5 (previously presented): The method of Claim 4, further comprising:

setting one of the plurality of condition code bits to indicate true if an associated compare condition is true and setting the one condition code bit to indicate false if the associated compare condition is false.

Claim 6 (previously presented): The method of Claim 1, further comprising:

converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

Claim 7 (previously presented): The method of Claim 6, wherein the first convert instruction is a CVT.PS.PW instruction.

Claim 8 (previously presented): The method of Claim 6, further comprising:

converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

Claim 9 (previously presented): The method of Claim 8, wherein the second convert instruction is a CVT.PW.PS instruction.

Claim 10 (previously presented): The method of Claim 1, wherein the floating point magnitude compare instruction is a CABS instruction.

Claim 11 (currently amended): A system that performs computer graphics view volume clipping comparisons to determine if a vertex is located within a specified view volume, the system comprising:

means for transforming a plurality of coordinates representing the vertex into a plurality of transformed coordinates; and

means for ~~performing a magnitude comparison, via~~ executing a floating point magnitude compare instruction to~~, between~~

determine an absolute value of at least one of the plurality of transformed coordinates and an absolute value that represents, for each respective at least one transformed coordinate, opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, and

perform a magnitude comparison between the absolute value of each of the at least one of the plurality of transformed coordinates and the absolute value of the corresponding view volume edges, wherein the magnitude comparison for each transformed coordinate involves a single comparison operation, and wherein comparison results for at least two view volume edges are obtained.

Claim 12 (previously presented): The system of Claim 11, further comprising:

means for setting a plurality of condition code bits to one or more specific states to indicate results of the magnitude comparison.

Claim 13 (previously presented): The system of Claim 11, further comprising:

means for specifying a compare condition in the magnitude compare instruction.

Claim 14 (previously presented): The system of Claim 13, further comprising:

means for setting one of the plurality of condition code bits to indicate true if an associated compare condition is true and setting the one condition code bit to indicate false if the associated compare condition is false.

Claim 15 (previously presented): The system of Claim 11, further comprising:

means for converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

Claim 16 (previously presented): The system of Claim 15, wherein the first convert instruction is a CVT.PS.PW instruction.

Claim 17 (previously presented): The system of Claim 15, further comprising:

means for converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

Claim 18 (previously presented): The system of Claim 17, wherein the second convert instruction is a CVT.PW.PS instruction.

Claim 19 (previously presented): The system of Claim 11, wherein the floating point magnitude compare instruction is a CABS instruction.

Claims 20-39 (previously canceled)

Claim 40 (previously presented): The method of Claim 1, wherein the plurality of coordinates and the plurality of transformed coordinates are in a paired-single data format.

Claim 41 (previously presented): The system of Claim 11, wherein the plurality of coordinates and the plurality of transformed coordinates are in a paired-single data format.

Claim 42 (previously presented): The method of Claim 1, wherein the floating point magnitude compare instruction is part of a general purpose instruction set architecture.

Claim 43 (previously presented): The method of Claim 1, wherein the floating point magnitude compare instruction is part of an application specific extension to a general purpose instruction set architecture.

Claim 44 (previously presented): The method of Claim 1, wherein the floating point magnitude compare instruction is executed in a single clock cycle.

Claim 45 (previously presented): The system of Claim 11, wherein the means for performing includes means for processing each of the at least one of the plurality of transformed coordinates in parallel.

Claim 46 (previously presented): The system of Claim 11, wherein the floating point magnitude compare instruction is part of a general purpose instruction set architecture.

Claim 47 (previously presented): The system of Claim 11, wherein the floating point magnitude compare instruction is part of an application specific extension to a general purpose instruction set architecture.

Claim 48 (previously presented): The system of Claim 11, wherein the floating point magnitude compare instruction is executed in a single clock cycle.